

What is claimed is:

- 1 1. A method of forming sidewall spacers adjacent opposing vertical sides of
2 a gate electrode, comprising:
3 forming at least one gate electrode over a substrate;
4 forming a first silicon oxide film conformally over the substrate and gate
5 electrode from a combination of gases including bis-(tertiarybutylamino)silane
6 and oxygen;
7 forming a silicon nitride film conformally over the first silicon oxide film
8 from a combination of gases including bis-(tertiarybutylamino)silane; and
9 forming a second silicon oxide film over the silicon nitride film from a
10 combination of gases including bis-(tertiarybutylamino)silane and oxygen.

- 2 2. The method of Claim 1, wherein forming the first silicon oxide film
3 comprises providing one or more wafers in a furnace at a first temperature, and
4 flowing BTBAS and oxygen into the furnace.

- 1 3. The method of Claim 2, wherein, forming the silicon nitride film, and the
2 second silicon oxide film comprises keeping the one or more wafers in the
3 furnace.

- 1 4. The method of Claim 2, wherein forming the silicon nitride film comprises
2 maintaining the one or more wafers in the furnace at a second temperature, and
3 flowing BTBAS and NH_3 into the furnace.

- 1 5. The method of Claim 4, wherein forming the second oxide film comprises
2 maintaining the one or more wafers in the furnace at the first temperature and
3 flowing BTBAS and oxygen into the furnace.

- 1 6. The method of Claim 4, wherein the first temperature is in the range of
2 550°C to 580°C, and the second temperature is in the range of 580°C to 600°C.

- 1 7. The method of Claim 1, further comprising, prior to forming the film silicon
2 nitride film and subsequent to forming the first oxide film, purging the furnace.

- 1 8. The method of Claim 7, wherein purging the furnace comprises ceasing
2 the flow of BTBAS and oxygen, and flowing N_2 into the furnace.

- 1 9. The method of Claim 1, further comprising, prior to forming the second
2 oxide film and subsequent to forming the silicon nitride film, purging the furnace.

- 1 10. The method of Claim 9, wherein purging the furnace comprises ceasing
2 the flow of BTBAS and NH_3 , and flowing N_2 into the furnace.

1 11. A method of forming a transistor, comprising:
 2 forming at least one gate electrode over a gate dielectric layer, the gate
 3 dielectric layer disposed on a substrate;
 4 depositing a first silicon oxide film conformally over the substrate and gate
 5 electrode from a combination of gases comprising bis-(tertiarybutylamino)silane
 6 and oxygen;
 7 depositing a silicon nitride film conformally over the first silicon oxide film
 8 from a combination of gases comprising bis-(tertiarybutylamino)silane and
 9 ammonia;
 10 depositing a second silicon oxide film over the silicon nitride film from a
 11 combination of gases comprising bis-(tertiarybutylamino)silane and oxygen; and
 12 forming a first sidewall spacer.

1 12. The method of Claim 11, wherein the first silicon oxide, the silicon nitride,
 2 and the second silicon oxide are deposited in-situ.

1 13. The method of Claim 11, wherein depositing the first silicon oxide, the
 2 silicon nitride, and the second silicon oxide are all done in a first furnace.

1 14. The method of Claim 13, wherein the first furnace is vertically oriented
 2 and the BTBAS, oxygen, nitrogen, and ammonia, each flow into the furnace from
 3 a bottom of the vertically oriented furnace.

1 15. The method of Claim 11, further comprising implanting dopants to form a
2 of deep source/drain region in the substrate adjacent at least two opposing sides
3 of the gate electrode.

1 16. The method of Claim 14, wherein forming a first sidewall spacer
2 comprises anisotropically etching the second silicon oxide layer, the silicon
3 nitride layer, and the first silicon oxide layer.

C3 sub B3
1 17. The method of Claim 16, further comprising removing the second oxide
layer so as to form L-shaped spacers.

C3 sub B3
1 18. The method of Claim 17, further comprising implanting dopants to form a
2 deep source/drain region in the substrate, adjacent to each opposing side of the
3 L-shaped spacers.

sub C4
1 19. The method of Claim 17, wherein implanting dopants includes a partial
2 passage of ions from an ion beam through a portion of the L-shaped spacers.

1 20. A field effect transistor, comprising:
2 a gate electrode overlying a gate dielectric layer disposed on a substrate;
3 a pair of L-shaped spacers adjacent opposing vertical sidewalls of the
4 gate electrode; and

5 a pair of source/drain regions disposed in the substrate and aligned,
6 respectively, adjacent to the pair of L-shaped spacers;
7 wherein each of the source/drain regions has a shallow tip portion
8 underlying each L-shaped spacer, a deep portion spaced away from the L-
9 shaped spacer, and an intermediate portion having a depth greater than that of
10 the shallow tip portion and less than that of the deep portion.

1 21. The field effect transistor of Claim 20, wherein each L-shaped spacer
2 comprises a silicon oxide layer immediately adjacent to the gate electrode.

1 22. The field effect transistor of Claim 21, wherein each L-shaped spacer
2 comprises a silicon nitride layer adjacent to the silicon oxide layer.

1 23. The field effect transistor of Claim 22, wherein the silicon nitride layer is
2 thicker than the silicon oxide layer.